IN THE SPECIFICATION:

Please rewrite the paragraphs at page 1, lines 15-32 to read as follows:

Fig. 1A depicts a partial top-view of a conventional MOSFET device 10. As shown in Fig. 1A, MOSFET device has a gate 12 over a substrate 22. A source region 14 and a drain region 16 are located in substrate 22 on opposite sides of gate 12. ~~Source and drain regions 14 and 16 are commonly~~ Gate 12 is referred to as having a length L that extends in the y-direction and a width W that extends in the z-direction, shown in Fig. 1A. Consistent with that usage, the dimension of a MOSFET gate, such as gate 12, in the z-direction, will hereafter be referred to as its width, and a reference to the ends of the gate will be understood to refer to opposite ends of the gate in the z-direction.

Fig. 1B is a cross-sectional schematic view of the MOSFET device 10. As shown in Fig. 1B, source 14 and drain 16 are formed in a well region 20 in substrate 22. Gate 12 is separated from substrate [[12]] 22 and thus source 14 and drain 16 by an oxide layer 15. The thickness of oxide layer 15 and the degree of any overlap of the gate over the source and the drain regions can vary. Device 10 may also have dielectric spacers 50 and 55 on two sides of gate 12, and lightly doped drain (LDD) regions 40 and 42 adjacent source and drain regions 14 and 16, respectively. Spacers 50 and 55 help to further isolate gate 12 from source 14 and drain 16 to prevent the build-up of device capacitance. Device 10 may be isolated from other devices also formed on substrate 22 by dielectric trenches (not shown) at some or all sides of device 10.